AMENDMENTS TO THE DRAWINGS

The attached sheet of drawings is a new drawing including FIG. 5 added after FIG. 4.

Attachment: New sheet of drawings including FIG. 5

REMARKS

The Examiner's Office Action dated December 7, 2005 has been received and its contents carefully considered.

In this Amendment, Applicants have amended the specification as shown above. Claim 11 has been canceled. Claims 1, 2, 5, 6, 8, 9, 16, 17, 18, 19, 20, 22, and 23 have been amended to specify the claimed invention, wherein claims 1, 5, 8, 9, 16, 17, 18, 19, and 22 are the independent claims. Claims 1-10 and 12-24 are now pending in the application. In addition, a new sheet of drawings including FIG. 5 is submitted. For at least the following reasons, it is submitted that this application is in condition for allowance.

The disclosure is objected to because of informalities on line 24 of page 7 indicated by the Office Action. In response, the informalities have been amended in accordance with the Examiner's indication. Thus, the objection should be respectfully withdrawn.

In addition, the drawings are objected to under 37 C.F.R. 1.83(a). In particular, the Office Action indicates that some terms in claims 1, 4, 8, 9, 16, and 17 must be shown or the features canceled from the claims, while no new matter should be added.

According to MPEP 2163.6 - Relationship of Written Description Requirement to New Matter, "*information contained in any one of the specification, claims or drawings of the*

application as filed may be added to any other part of the application without introducing new matter." Thus, with the support from the claims (e.g. claims 1, 4, 8, and 9) and detailed description (e.g. paragraphs beginning at line 27 of page 8, and lines 18-24 of page 9) of the originally filed application, Applicant respectfully requests a new sheet of drawings -FIG. 5- to be added to the application after FIG. 4. Applicant has also added a new paragraph after the paragraph beginning at line 18 of page 6, and has amended the paragraphs beginning at line 21 of page 6, line 27 of page 8, and line 18 of page 9 in order to meet the provisions and requirements indicated by the Office Action. In particular, FIG. 5 is being added with at least the support of claims 1, 4, 8, and 9, and the passage of lines 18-24 of page 9, where it is recited that "[A]lternatively, the test transistors NL1~NL4 may have drains/sources coupled to the data signal lines 26 instead of the scan signal lines 24, or, in addition to the test transistors NL1~NL4, there may be test transistors having drains/sources coupled to the data signal lines 26." It is submitted that the terms indicated by the Office Action in the objection are either indicated in FIG. 4 or 5 or supported by the amended paragraphs, with the support of the originally filed application. Therefore, it is respectfully submitted that the objection be withdrawn.

Claims 1-24 stand rejected under 35 U.S.C. 102(e) as being anticipated by Kodate et al. (U.S. Patent No. 6,784,862; hereinafter "Kodate"). Since claim 11 has been canceled, the rejection of claim 11 is rendered moot. Claims 1, 5, 8, 9, 16, 17, 18, 19, and 22 are the independent claims. It is submitted that claims 1-10 and 12-24 are not anticipated or rendered obvious over the cited reference for at least the following reasons.

It is well settled that a reference may anticipate a claim within the purview of 35 USC section 102 only if all the features and all the relationships recited in the claim are taught by the reference structure either by clear disclosure or under the principle of inherency.

Applicants' independent claim 1, as amended, recites "*[a]n active matrix display device having a display region consisting of sub-pixels arrayed in a matrix fashion, the sub-pixels having switching elements, comprising: a plurality of data signal lines for sending data signals to the sub-pixels; a plurality of scan signal lines for sending scan signals to the sub-pixels;* ***a plurality of common voltage lines for sending a reference voltage to the sub-pixels; first test transistors, each of which is connected to one of the plurality of scan signal lines for sending first test signals thereto;*** *and a plurality of first input terminals, each of which is connected to one of a plurality of the first test transistors; wherein* ***each gate of the first test transistors and each of the common voltage lines are connected*** *to one of the first input terminals, the first test transistors control inputs of the first test signals to the sub-pixels*"(emphasis added).

That is, the display device of claim 1 includes **three different types of lines for sub-pixels: the data signal lines, scan signal lines, and common voltage lines**. In addition to the sub-pixels of the display region, the display device includes **first test transistors, which control inputting of the first test signals to the sub-pixels** and **whose gates are coupled to the common voltage lines**. It is submitted that Kodate does not disclose or

even suggest the common voltage lines, the test transistors, and the relationship among the common voltage lines and test transistors, as claim 1 requires.

The Office Action asserts that Kodate discloses the common voltage lines (11) since "the scan signal lines (11) are also considered as the common voltage lines (11)." Applicant respectfully disagrees. It is submitted that Kodate does not disclose or even suggest the common voltages lines, which are coupled to the gates of the test transistors, as claim 1 requires. Instead, Kodate discloses that **the test TFTs 22** whose drain electrodes 24 are connected to the scan signal lines 11 **have their gate electrodes 25 connected to a line of the inspection circuit 5** which is connected to a test terminal 35 (See FIG. 5 of Kodate), and **such line of the inspection circuit 5 is not the asserted "common voltage line" (11)** and **is isolated from the asserted "common voltage line" (11)**. If the scan signal lines (11) of Kodate were the common voltage lines, as asserted by the Office Action, Kodate would disclose that the common signal lines (11) were connected to the gate electrodes of the test TFTs 22, as Applicant's claim 1 requires. However, such structural relationship was not disclosed or even suggested among the asserted "common voltage lines" (11) and the test TFTs 22.

As such, the claimed structure is not disclosed, nor is it suggested, by Kodate. Thus, claim 1 is not anticipated, or rendered obvious, by the cited reference.

Moreover, it is noted that the Office Action asserts that the other independent claims 5, 8, 9, 16, 17, 18, 19, and 22 include similar claim elements and limitations recited in claim 1 and thus rejects these claims based on the same reason as applied to claim 1. Therefore, for at least the reasons as to the discussions of the patentability of claim 1 as well as additional features recited in the claims rejected, it is respectfully submitted that these independent claims, as well as their respective dependent claims, are also not anticipated or rendered obvious by the cited reference.

For example, regarding independent claim 18, the disclosure of "*when driving the display device by scan signals and data signals, applying a reference signal indicating disabling the test switches to the control terminals of the test switches to disable the test switches while the reference signal serves as a common voltage to be supplied on the common voltage lines so as to enable storage capacitance to be formed within the sub-pixels*" is not anticipated or rendered obvious by the cited reference.

Regarding independent claim 19, the recitation that "*the test transistors are turned on by the second signal so that the first signals are transmitted on the first lines to drive the pixels during a test, and the test transistors are turned off by the second signal so that the first signals are isolated from the first lines and the second signal is used as the common voltage supplied to the pixels through the third lines beyond the test*" is not anticipated or rendered obvious by the cited reference. Should the Examiner disagree with the Applicant,

the Examiner is respectfully requested to show where, in the cited reference, such limitation is shown.

Conclusion

For the foregoing reasons, it is respectfully submitted that this application with claims 1-10 and 12-24 is in condition for allowance. Notice of such allowance and passing of the application to issue, are earnestly requested.

Should the Examiner feel that a conference would be helpful in expediting the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

The Commissioner is authorized to charge any additional fees, which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Post Office with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendments, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 on

March 7, 2006
(Date of Transmission)

Susan Papp
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03/07/06
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Respectfully submitted,

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Encls.: New Sheet 1/1 (Figure 5)
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